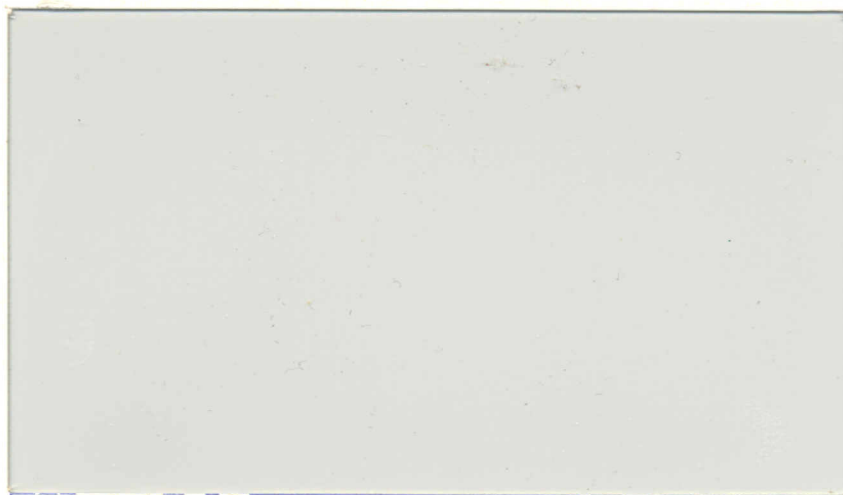




QBX-FOG/E

HARDWARE STACK
AND
NON-VOLATILE EEPROM

USER MANUAL

QBX÷FOG/E

Product:÷ QBX÷FOG/E

Product Number:÷ 1102(÷256), 1202(÷64)

Manual Number:÷ 1002÷01

Chapter	Rev	Note
All	1.0	1
1,4	1.1	2
2,5	1.1	3

Notes:÷

1.Original Document

2.Spelling corrections,R&D Elec/Quantum change, R & D new phone

3.Addition at end of chapter 2, and change of PAL number in 5.

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Rev:1.2

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CHAPTER 1 GENERAL

Introduction

The QBX-FOG/E board is one of a growing range of iSBX bus compatible boards manufactured by R & D Electronics. These boards are designed to increase the number of functions on a Multibus system without having to resort to the addition of a full sized Multibus card to achieve that function. This document provides all the information required to use the QBX-FOG/E.

Description

The QBX-FOG/E takes full advantage of the latest developments in the field of EEPROM (Electrically Erasable and Programmable Read Only Memory) Technology, to provide a means of up to 256 bytes of non-volatile storage on the SBX bus. In addition the memory is configured as a stack allowing extra flexibility in user software.

The stack has two parts; an ordinary RAM (Random Access Memory) and a bit for bit "shadow EEPROM". In fact both these devices are contained on a single chip entitled "NOVRAM" (NO n Volatile RAM) made by Xicor Inc. Access to the RAM is by "pushing" and "popping" as with a normal stack. Any address in the memory range may be set as the starting address. At any point during the user programme the contents of the RAM may be transferred to the EEPROM overwriting the original contents. Alternatively at any stage the EEPROM may be recalled into RAM overwriting the RAM contents.

Programming the EEPROM only requires a 5 volt supply and no standby voltage is required during power down.

Equipment Supplied

The QBX-FOG/E is shipped in a padded package. Included in this package are a plastic spacer and two plastic screws to mount the QBX board onto the host SBC Computer.

The QBX-FOG/E-64 has 64 bytes of NOVRAM on board, whilst the QBX-FOG/E-256 has 256 bytes. The difference occurs with the type of NOVRAM chips used.

Specifications

Access Time:

Read and write address 100nS
Read stack 400-600nS
Array recall 800-1000nS
Array save 100nS
Write stack 150nS

Addressing Range:

The QBX-FOG/E is compatible with any board that supports the Intel iSBX bus. The addressing range of the QBX-FOG/E is derived from this host board.

Interface:

System Bus Compatible with the SBX bus specifications. See Intel publication 142686-001

Power Requirements:

+5 Volt -2%,+5% @545mA

Environment:

Operating temperature 0-55 degrees Celsius, humidity to 90% non-condensing.

Size:

Width 724 mm (2.85 in)
Length 943 mm (3.71 in)
Height 19.4mm(0.76 in) including QBX connector

CHAPTER 2 PRINCIPLE OF OPERATION

Introduction

This chapter describes the operation of the QBX-FOG/E. Appendix B contains extracts of the X2212-30, the NOVRAM that forms the heart of the QBX-MSP/4.

Overview

The NOVRAM is a device that contains RAM and a bit for bit "shadow" EEPROM. A diagrammatic representation of a 64 x 4 bit device is shown in figure 2.1

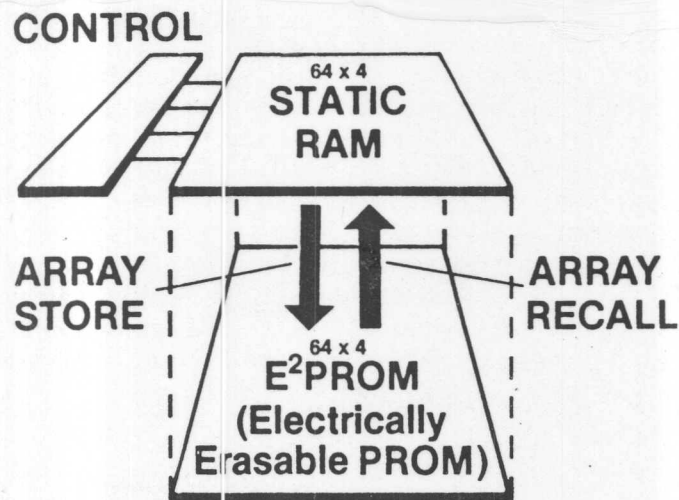


Figure 2.1
Pictorial Representation of NOVRAM
(c) copyright 1981 Xicor Inc used with permission.

An electrical signal will cause the data to move in either direction as shown by the arrows in figure 2.1. All signals are TTL compatible and no power supply is required for retention of the data in the EEPROM during power down. The transfer of data from the RAM array to the EEPROM array overwrites all the data in the latter whilst the former remains unchanged. The converse is also true.

Since the SBX bus is essentially an I/O bus it is not a straightforward matter to access 256 bytes, as this requires 8 bits of

addressing. To solve this problem the QBX-MSP/E is configured as a stack. This stack is in addition to the normal microprocessor stack. Whilst the original intention was to provide an easy way of accessing the NOVRAM, there is considerable advantage (from a software viewpoint) in having an extra stack.

QBX Bus Interface

Detailed description of the iSBX bus is contained in the Intel publication 142686-001. Users are referred to this document for a clearer understanding of the signals. The QBX-FOG/E uses the following signals: MD0-MD7, MA0-MA2, IORD/, IOWR/, CS0/, CS1/, MRESET, MCLK, MWAIT and of course MPST/, +5 volts, and ground.

Circuit Description

All address decoding is achieved via a PAL (programmed array logic) that has been customised for this task. There are 6 functions on the QBX-FOG/E. They are:

- (i) Set stack address
- (ii) Read stack address
- (iii) Write to RAM
- (iv) Read from RAM
- (v) Save array (RAM -> EEPROM)
- (vi) Recall array (EEPROM -> RAM)

Wait state generation:

Actions (iv) and (vi) require extended timing due to certain conditions that will be described later. To achieve this wait states of varying lengths are generated. The 10 MHz MCLK signal is divided by 2 (N4) and fed to the clock of a serial to parallel shift register (N3). The data inputs to this device are held high, and the reset signal is normally held active keeping the data outputs at a zero. When a read to the RAM is executed the WAITEN/ line goes active (N1/14) and the COUNTDOWN/ signal goes low. This enables both the shift register (which shifts a "1" onto successive outputs every 200ns) and the input to a NAND gate (N5/11). The open collector output of this device goes low forcing a wait condition on the processor until QC of the shift register (N3#/5) goes high, 400-600ns later.

The wait condition on array recall is similar except that COUNTDOWN/ remains high, enabling the alternate NAND gate which generates a wait state length of 800-1000ns.

Stack address:

The stack address is generated by using two up/down programmable counters, the 74LS193 (N7,N8). The outputs of these counters drive the address input of the NOVRAM chips. Setting up the stack pointer is merely a matter of writing to the addresses XF hex, X depends on the host computer.

The value of the counter may be read at any time without affecting its value by reading from the stack read address XF hex, X depends on the host computer.

Push:

Writing to the RAM constitutes a push operation. The data on the data bus is stored at the address on the counters. The trailing edge of the write pulse clocks the count up input of the counters setting up the new address for the next operation. The address that must be written to is X0 hex, X is determined by the host board.

The counters loop from FF to 00 on count up, and from 00 to FF on count down.

Pop:

Reading from the RAM constitutes a "pop" action. As mentioned above when address X1 hex is read from COUNT DOWN/ goes low. This triggers a monostable N2, forcing the Q/ output low. At the end of the monostable period this Q/ signal clocks the count down signal. The counters are decremented and the contents of the new address are allowed onto the bus. The propagation delays of this process necessitate wait state generation.

Array Recall:

An array recall requires a signal of 750nS on pin 10 of the NOVRAM. A read signal to address X2 hex satisfies this requirement.

Array Save:

In order to transfer the contents of the RAM to the EEPROM a read at address X3 hex must be executed.

NOTE:

Data retention in the EEPROM is indefinite.

Any number of Array recall cycles is permitted.

There are a limited number of storage cycles. This number is guaranteed at 1000 while it is typically 5000.

Power Fail and Reset:

When power falls below 4.5 volts nominal an array recall is executed as an array save is thus excluded. This protects the integrity of the data in the EEPROM. Further a MRESET signal will also generate an array recall for similar reasons of protecting the data until the microprocessor has reached a known condition. The reset signal also sets the stack counter to 00.

Note

Whilst an array recall is generated on reset, a software array recall must be executed to guarantee the correct results.

CHAPTER 3 PROGRAMMING INFORMATION

Introduction

This chapter describes the programming and possible applications of the QBX-FOG/E. Appendix A deals with an application.

Stack Counter

Setting up the stack counter is merely a case of writing the wanted address to address XF hex, X determined by the host board. For example, to programme address 57 hex on the stack address, with the QBX memory space on the host board C0 to CF hex, an assembly programme would appear similar to the following:

```
MVI A,57H
OUT 0CFH
```

Reading this back is a Read to this location e.g.

```
IN 0CFH
```

Push

In order to save information in the RAM a push sequence must be executed. The byte that is required to be stored is written to location X0 hex. It is stored at the address contained on the counters. At the termination of the write the counters are incremented by 1. To store 98 on the stack with the same conditions as the above example:

```
MVI A,98          ;stack counter at 34 hex,say
OUT 0C0H          ;stack counter at 35 hex
```

Pop

To extract information from the RAM, a Read from the RAM is executed. The information at the current counter address -1 is read. e.g.

```
IN 0C0H          ;stack counter at 35 hex
                  ;information from 34 hex on accumulator
```

NOTE:

Pushing at FF hex rolls the counters over to 00. Popping at location 00 reads the contents of location FF hex. The maximum address on the QBX-FOG/E-64 is 3F hex. The two most significant bits of the counter have no effect, except the counters are still capable of 256 distinct values.

Array Recall

After execution of this instruction all previous contents of the RAM are lost and overwritten by the contents of the EEPROM. The contents of the stack counter are unaffected. The contents of the RAM cannot be read for a period of 1.5uS after this, but this should not be a problem. e.g to array recall

```
IN    0C2H                ;contents of EEPROM now in RAM
```

Array Save

In order to save the RAM array onto the EEPROM a read at location X3 hex is executed. All contents of the EEPROM are lost and overwritten by the contents of the RAM. The contents of the stack counter remain unchanged.

IMPORTANT NOTE. Whilst the actual save process is fast (100ns) any action on the RAM before 10ms is up can produce erroneous results.

```
IN    0C3H                ;array recalled
CALL WAIT                ;10ms wait if next action acesses
                                ;or array recalls NOVRAM
```

Summary of Functions and Addresses

Table 3.1 provides a summary of the functions and their associated addresses on the QBX-FOG/E.

Binary Add.	Read	Write	Counter	Action
ABCD1111		@	Data -> Counter	Load stack counter
ABCD1111	@		Counter -> Data	Read stack counter
ABCD0010	@		No change	EEPROM array to RAM
ABCD0011	@		No change	RAM to EEPROM array
ABCD0001	@		N -> N-1	Read byte at location N-1. "POP".
ABCD0000		@	N -> N+1	Write byte to location N. "PUSH".

Note:

ABCD is a binary number determined by the host computer where A is the most significant bit of the 8 bit number.

@ = active.

Table 3.1
Summary of Functions and their Associated Addresses

The QBX-FOG/E is configured as a hardware stack, similar to the stack on any microprocessor. Most microprocessors (and certainly the 8085/Z80) only allow for a single stack in their architecture. As a result, passing parameters on a CALL instruction, and managing these when these routines need to be reentrant can be complicated. The QBX-FOG (both FOG/C and FOG/E) can aid in this situation.

Since the stack counter is also programmable, several stacks may be maintained for different routines. As the value of the stack counter may be read back, information may also be conveyed here. If for example the parameters passed are characters in a message of variable length to be output to a Visual Display Unit, then the message is complete when the stack counter reaches the original value at the time of passing the parameters. (See Appendix A).

The EEPROM feature allows for say, on power up loading certain parameters and then using the stack as above, ignoring the presence of the EEPROM.

An EEPROM provides the capability to "customise" a system on site and also allows the computer to store parameters it has learnt about its environment.

The NOVRAM structure allows an EEPROM with a bit change capability. e.g. ARRAY RECALL, modify bit, and ARRAY SAVE.

The potential of the QBX-FOG/E is limited only by the designer's imagination.

CHAPTER 4 PREPARATION FOR USE

Introduction

This chapter provides information on the installation of the QBX-FOG/E on a host SBC board.

Unpacking

The QBX-FOG/E is shipped in a padded packet together with 1 plastic spacer and 2 plastic screws.

On receipt of the package inspect immediately for signs of damage, water or any other signs of mishandling. If there are any of these signs contact your carrier or his agent, or the local R & D Electronics representative. If you do open the package, please retain the packaging.

Mounting

The QBX-FOG/E will mount on any SBC computer that allows an iSBX board. Affix the spacer with one of the screws to the host board. Mount the spacer in the hole corresponding to the only hole on the QBX board.

The QBX-FOG/E should now be mounted on the mating connector and affixed to the host board with the remaining screw.

When a QBX card is mounted on a host card, the resulting structure occupies an additional card slot above the SBC card. Bear this in mind when you allocate slots in a cardframe.

CHAPTER 5 SERVICE

Introduction

This chapter provides a parts list and a schematic diagram of the QBX-FOG/E

Parts List

Semiconductors:

N1	programmed part	PAL 16L8
N2	monostable multivibrator	74121
N3	serial to pll s.r.	74LS164
N4	dual D-type flip flop	74LS74A
N5	o.c. 3 input NAND gate	74LS12
N6	octal buffer	74LS245
N7,8	prog. up/dwn counter	74LS193
N9,10	NOVRAM FOG/E-255	X2212-30
	NOVRAM FOG/E-64	X2210-30
N11	hex o.c. buffer	7417
N12	hex inverter	74LS04
Q1,2	general NPN transistor	BC107
Z1	400 mW zener diode	3V9

Capacitors:

C3-5	ceramic	0.001uF
C2	ceramic	470pF

Resistors:

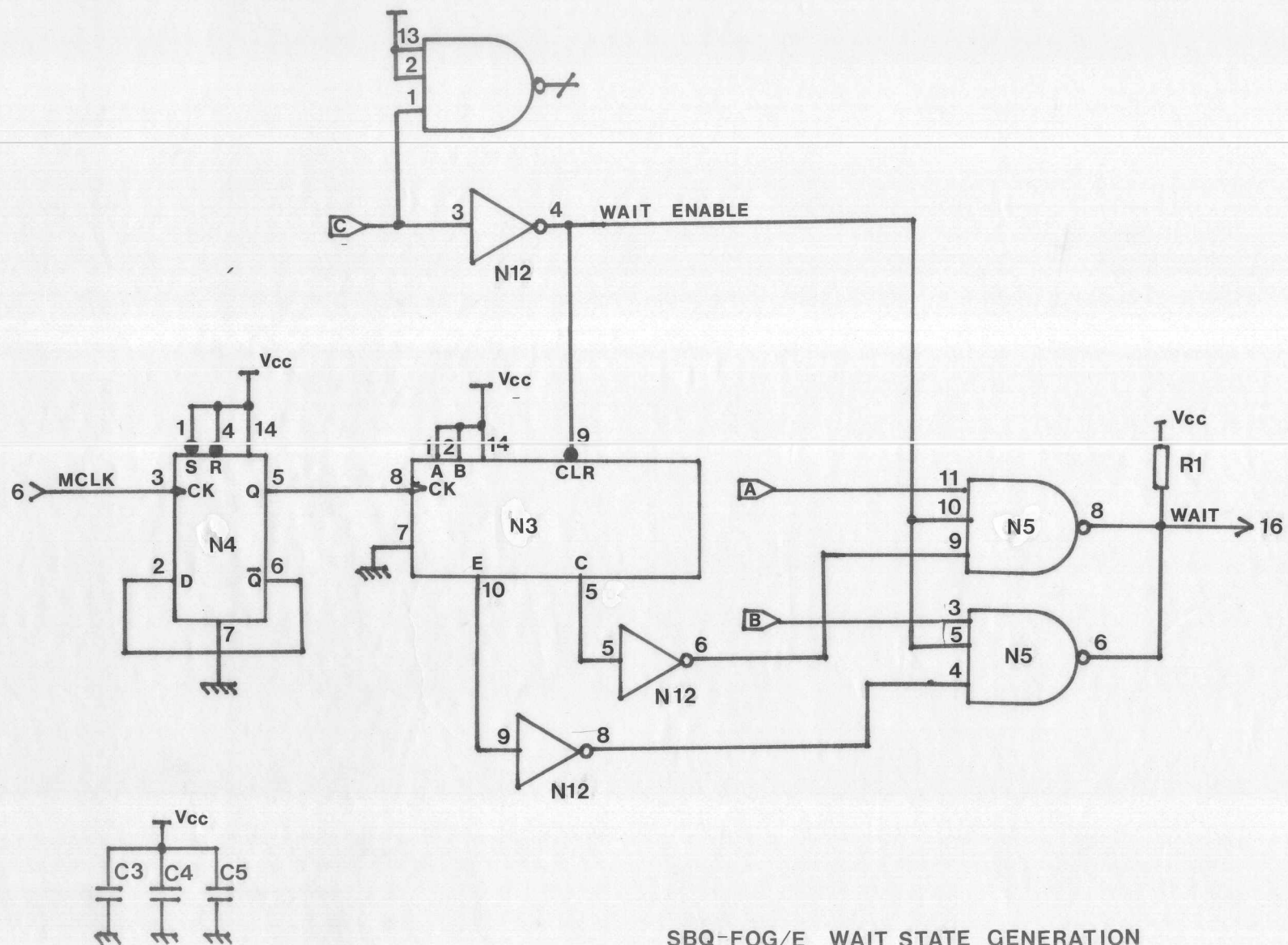
R1	1/4W 2%	2K2
R2	1/4W 2%	1K0
R4	1/4W 2%	33
R5	1/4W 2%	100
R6,8	1/4W 2%	1K2
R7	1/4W 2%	10K0
R9	1/4W 2%	10

Connector:

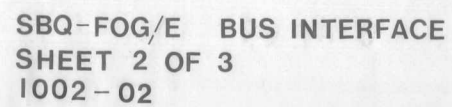
36 way SBX	LMP01KH18A01
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Unused parts:

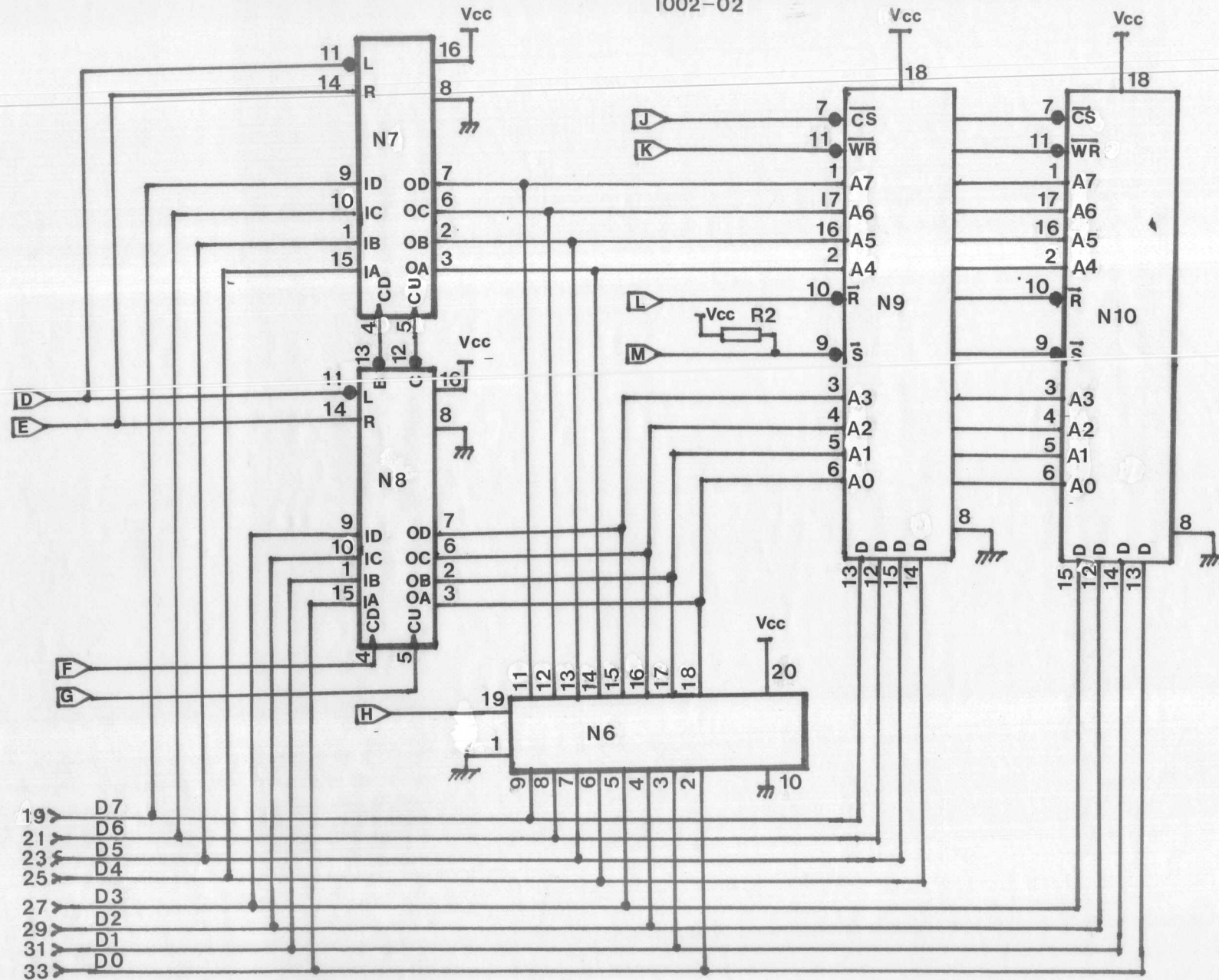
C1
R3



SBQ-FOG/E WAIT STATE GENERATION
 SHEET 1 OF 3
 1002-02
 Rev: 1.0



SBQ-FOG/E LIFO STACK
SHEET 3 OF 3
1002-02



APPENDIX A A CASE STUDY

A project requires (amongst other things) that a computer monitor the level of a liquid in a container. The transducer used to measure the level suffers from drift and so the computer conversions must be calibrated. The output from the transducer is however, linear. Certain messages are also to be transmitted to a resident Visual Display Unit (VDU) informing of the system status.

Use of the QBX-FOG/E allowed the following solution. At installation, (and every time calibration is required) known quantities of liquid are added to the container. The corresponding output levels are measured by the computer and interpreted to provide an equation of the transducer output related to the quantity of liquid. The parameters of this equation are then saved in EEPROM.

On power up or reset the EEPROM is loaded to the stack and the parameters are loaded to RAM allowing the stack of the FOG/E to be used for the following purpose.

To output a variable length message to the VDU the setup routine pushes the message to be transmitted in reverse order onto the stack, starting at location 00. As each character is transmitted the microprocessor "pops" the next byte off the stack and checks to see if the stack counter is back at zero. It transmits this byte and if the counter was at zero then the message is completely transmitted and the computer can terminate this process.

Summary

Parameters of any nature can be stored and modified in the above fashion on site. The stack adds a feature that is not often seen on microcomputer boards.

APPENDIX B
X2212 NOVRAM Data Sheet

The following pages are extracted from the X2212 data sheet. The X2212 is a 256x4 device used on the FOG/256. The X2210 is a 64x4 device used on the FOG/E-64. The only difference is that address pins A6 and A7, (pins 1 and 17) are not connected on the package.

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10% Power Supply Margin
 $V_{CC} = 5V \pm 10\%$

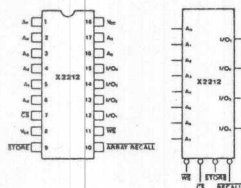
256 x 4 Bit Nonvolatile Static RAM
5V-Programmable

X2212

- NONVOLATILE STATIC RAM:** The X2212 contains 2K bits of memory organized as a conventional 1K static RAM overlaid bit-for-bit with a nonvolatile 1K Electrically Erasable PROM (E²PROM). Nonvolatile data can be stored in the E²PROM and at the same time independent data can be accessed in the RAM memory. At any time, data can be transferred back-and-forth between the RAM and E²PROM by simple store and array recall signals.
- 5V-PROGRAMMABLE:** High-voltage pulses or supplies are never required. A single 5V supply is the only power source ever required for any function.
- EASE-OF-USE:** Unprecedented simplicity, all inputs and outputs are directly TTL compatible. Fully static timing, 18-pin package.
- PERFORMANCE:** RAM cycle time is less than 300 ns. During the lifetime of the device, data can be recalled from the E²PROM an unlimited number of times.
- POWER-FAILURE PROTECTION:** One simple TTL signal saves the entire RAM database. A snapshot nonvolatile copy of all RAM data is internally stored safe without power and can be recalled to the RAM when power returns. No battery backup required.
- ORGANIZED FOR MICROCOMPUTER SYSTEMS:** The common data input and output is organized four bits wide.

Xicor's X2212 is fabricated with reliable n-channel floating gate MOS technology. For systems where RAM nonvolatility or in-the-circuit ROM changes by TTL signals are important, the Xicor X2212 is an ideal choice.

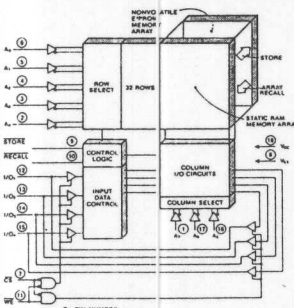
PIN CONFIGURATION
18 PIN DIP .300"



PIN NAMES

A ₀ - A ₇	ADDRESS INPUTS
I/O ₀ - I/O ₃	DATA INPUT/OUTPUT
WE	WRITE ENABLE
CS	CHIP SELECT
AR	ARRAY RECALL
S	STORE
V _{CC}	+5V
GND	GROUND
NC	NO CONNECT

FUNCTIONAL DIAGRAM X2212 (256 x 4)



©XICOR, 1981 Patents pending.
Advanced data sheet effective September 1981.
Stock No. 200-004

XICOR, Inc., 851 Buckeye Court, Milpitas, California 95035 (408) 946-6920 TWX 910-379-0033

X2212

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-10°C to +85°C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-1.0V to +6V
D.C. Output Current	5mA

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

X2212 D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ± 10%, unless otherwise specified.

Symbol	Parameter	Min	Typ ⁽¹⁾	Max	Units	Test Conditions
I _{CC}	Power Supply Current		40	60	mA	All Inputs = 5.5V I _{OQ} = 0mA T _A = 0°C
I _I	Input Load Current		1	10	μA	V _{IN} = GND to 5.5V
I _{LO}	Output Leakage Current		1	10	μA	V _{OUT} = GND to 5.5V
V _{IL}	Input Low Voltage	-1.0		.8	V	
V _{IH}	Input High Voltage	2.0		V _{CC}	V	
V _{OL}	Output Low Voltage		.4		V	I _{OL} = 4.2mA
V _{OH}	Output High Voltage	2.4			V	I _{OH} = -2mA

CAPACITANCE

T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max	Unit	Conditions
C _{IO}	Input/Output Capacitance	5	pF	V _{IO} = 0V
C _{IN}	Input Capacitance	5	pF	V _{IN} = 0V

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0 Volt to 3.0 Volt
Input Rise and Fall Times	10 nsec
Input and Output Timing Levels	1.5 Volts
Output Load	1 TTL Gate and C _L = 100 pF

TRUTH TABLE

INPUTS				INPUT/OUTPUT	MODE
CS	WE	ARRAY RECALL	STORE	I/O	
H	X	H	H	Output High Z	Not Selected ⁽¹⁾
L	H	H	H	Output Data	Read RAM
L	L	H	H	Input Data High	Write "1" RAM
L	L	H	H	Input Data Low	Write "0" RAM
X	H	L	H	Output High Z	Array Recall
X	H	H	L	Output High Z	Nonvolatile Storing ⁽²⁾
H	X	H	L	Output High Z	Nonvolatile Storing ⁽²⁾

- NOTES: (1) Chip is deselected but may be automatically completing a store cycle.
(2) STORE = L is required only to initiate the store cycle, after which the store cycle will be automatically completed (STORE = X).
(3) Typical values are for T_A = 25°C nominal supply voltages.

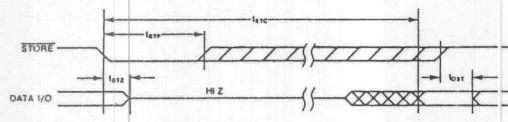
2

X2212

STORE CYCLE

Symbol	Parameter	Min	Typ ⁽¹⁾	Max	Units
t _{STC}	Store Cycle Time		10		ns
t _{STP}	Store Pulse Width	100			ns
t _{STZ}	Store to Output in High Z			100	ns
t _{OST}	Output Active from End of Store	10			ns

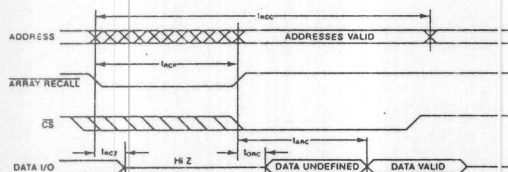
NUMBER OF STORE CYCLES: Based on presently available data, the X2212 is expected to perform typically 5,000 valid store cycles. A minimum number of 1,000 valid store cycles is specified.



ARRAY RECALL CYCLE

Symbol	Parameter	Min	Typ ⁽¹⁾	Max	Units
t _{ARC}	Array Recall Cycle Time	1200	1000		ns
t _{ARP}	Recall Pulse Width	450			ns
t _{ARZ}	Recall to Output in High Z			100	ns
t _{ORC}	Output Active from End of Recall	10			ns
t _{ARC}	Recalled Data Access Time from End of Recall			750	ns

NUMBER OF RECALL CYCLES: After data has been stored properly in the nonvolatile memory (E²PROM), the X2212 is expected to recall this data an unlimited number of times during the lifetime of the device.



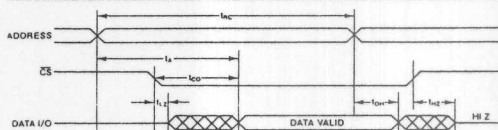
X2212

X2212 A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ± 10%, unless otherwise specified.

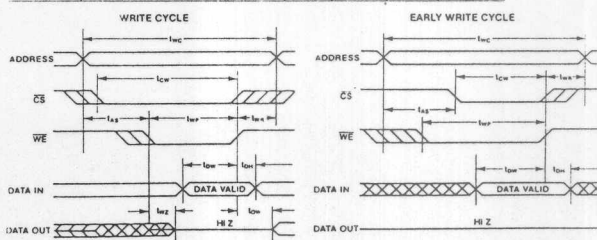
READ CYCLE

Symbol	Parameter	Min	Typ ⁽¹⁾	Max	Units
t _{RC}	Read Cycle Time	300			ns
t _A	Access Time			100	ns
t _{CO}	Chip Select to Output Valid			200	ns
t _{OH}	Output Hold from Address Change	50			ns
t _{LZ}	Chip Select to Output in Low Z	10			ns
t _{HZ}	Chip Deselect to Output in High Z	10		100	ns



WRITE CYCLE

Symbol	Parameter	Min	Typ ⁽¹⁾	Max	Units
t _{WC}	Write Cycle Time	300			ns
t _{CW}	Chip Select to End of Write	150			ns
t _{AS}	Address Set-up Time	50			ns
t _{WP}	Write Pulse Width	150			ns
t _{WR}	Write Recovery Time	25			ns
t _{DW}	Data Valid to End of Write	100			ns
t _{DH}	Data Hold Time	20			ns
t _{WZ}	Write Enable to Output in High Z	10		100	ns
t _{OW}	Output Active from End of Write	10			ns



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X2212 DEVICE OPERATION

ADDRESSES (A₀-A₇):

The eight address inputs select one of the 256 4-bit words.

CHIP-SELECT ($\overline{CS}$):

The chip select terminal affects the data-in/data-out and write enable terminals. When chip-select is high, the I/O terminals are in the floating or high impedance state.

WRITE ENABLE ($\overline{WE}$):

RAM READ/WRITE CYCLES

The RAM read or RAM write mode is selected through the write enable terminal when $\overline{CS}$ is low. A logic high selects the RAM read mode; a logic low selects the RAM write mode.

STORE ($\overline{\text{STORE}}$):

NONVOLATILE E²PROM WRITE CYCLE

Modification of data in the E²PROM memory is controlled by the STORE terminal. A low logic STORE signal applied to a device defines a store cycle which transfers a complete 256 x 4-bit copy of all 256 x 4-bit RAM storage locations into the corresponding 1024-bit locations of the overlaid nonvolatile E²PROM memory. The data in the E²PROM has been modified and is a "snapshot copy" of the current RAM data. The original data in the RAM remains valid. A low logic STORE signal initiates an automatic internal store operation. A low logic STORE into a device also inhibits write enable and array recall: data-in/data-out terminals are in a high impedance state. The inhibited terminals are enabled by either automatic completion of the internal store operation or upon a high logic STORE, whichever is longer. A store cycle can take place when CS is high or low. Data stored in the E²PROM remains valid with or without power supplied.

Care must be taken to prevent an unintentional initiation of a store cycle during power-up and power-down. A low logic ARRAY RECALL will inhibit the initiation of a STORE operation. In many microcomputer systems the system reset command can be used during power-up and power-down to generate a low ARRAY RECALL. Another means of assuring a store cycle will not be initiated during power-up or power-down is to keep STORE high, for example by tying the input through a pullup resistor to V_{CC} , to assure that STORE approximately equals V_{CC} . In addition, the STORE operation is inhibited for V_{CC} approximately less than 3 volts.

ARRAY RECALL (ARRAY RECALL):

NONVOLATILE E²PROM READ CYCLE

Nonvolatile data stored in the E²PROM is copied back into the RAM by the ARRAY RECALL terminal. Once the E²PROM data is back in the RAM it can then be accessed by normal RAM read or write cycles. A low logic ARRAY RECALL into a device initiates a cycle that in a single operation transfers the entire 1024-bit E²PROM array data bit-for-bit into the 1024-bit RAM memory. The E²PROM data overwrites any data then existing in the RAM at the beginning of an ARRAY RECALL cycle. The data in the E²PROM remains unaltered.

A low logic ARRAY RECALL inhibits the STORE terminal. An array recall cycle can take place when CS is high or low.

DATA-IN/DATA-OUT (I/O₁-I/O₄):

Data can be written into the RAM section of a selected device when the write enable input is low. The three-state output buffer provides direct TTL compatibility. The I/O terminals are in the high impedance state when chip select is high or whenever a write operation is being performed.

PACKAGING INFORMATION

